IN THE CLAIMS

1. (Currently Amended) A method of routing IP packets between a plurality of circuit cards within a node of a network, comprising:

receiving a packet at an interface, the packet being an IP packet and including a label stack, the label stack including an external routing label for use in forwarding between nodes along a label-switched path;

pushing an internal routing label to the label stack of the packet, the ~~examining a packet, the packet including an~~ internal routing label specifying one of a plurality of circuit cards and a packet type;

routing the packet to the one of the plurality of circuit cards specified in the internal routing label in response to the packet type being indicative of a first type.

2. (Currently Amended) The method, as set forth in claim 1, wherein routing the packet to the one of the plurality of circuit cards comprises routing each packet to [[~~by~~]] at least a shelf and slot numbers included in the internal routing label.

3. (Previously Presented) The method, as set forth in claim 1, wherein routing the packet to the one of the plurality of circuit cards comprises routing each packet based on a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label.

4. (Currently Amended) The method, as set forth in claim 32 [[~~1~~]], wherein sending the reply packet to ~~a sender~~ one of the plurality of circuit cards comprises routing the reply packet to the one of the plurality of circuit cards based on shelf and slot numbers included in the routing label.

5. (Previously Presented) The method, as set forth in claim 32, wherein sending the reply packet to the one of a plurality of circuit cards comprises routing the reply packet based on a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label for transporting the reply packet.

6. (Previously Presented) The method, as set forth in claim 1, wherein routing the packet to the one of a plurality of circuit cards comprises:

receiving the packet at a switch; and

switching the packet to the one of a plurality of circuit cards coupled to a predetermined port of the switch as specified by shelf and slot numbers of the destination included in the internal routing label.

7. (Previously Presented) The method, as set forth in claim 1, wherein routing the packet to the one of a plurality of circuit cards comprises:

receiving the packet at a switch; and

routing the packet to the one of a plurality of circuit cards coupled to a predetermined port of the switch as specified by a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label.

8. (Previously Presented) The method, as set forth in claim 32, wherein routing the packet to a processor and sending the reply packet comprises:

receiving the packet at a switch;

switching the packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet to the one of the plurality of circuit cards coupled to a second predetermined port of the switch specified by shelf and slot numbers included in the internal routing label.

9. (Previously Presented) The method, as set forth in claim 32, wherein routing each packet to a processor and sending the reply packet to one of the plurality of circuit cards ~~a sender~~ comprises:

receiving each packet at a switch;

switching the packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet to the one of the plurality of the circuit cards coupled to a second predetermined port of the switch specified by a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label for transporting the reply packet.

10 -11. (Cancelled)

12. (Currently Amended) The method, as set forth in claim 1, further comprising popping the internal routing label from ~~a~~ the label stack on the packet after receiving the packet at the one of the plurality of circuit cards.

13. (Previously Presented) The method, as set forth in claim 32, further comprising popping the routing label from the label information table stack after receiving the packet at the processor within the system.

14-22. (Cancelled)

23. (Previously Presented) The method, as set forth in claim 1, further comprising pushing the internal routing label onto a label stack of the packet after receiving the packet.

24. (Cancelled)

25. (Previously Presented) The method, as set forth in claim 23, further comprising popping the routing label from the label stack after receiving the packet at the processor within the node.

26 – 27. (Cancelled)

28. (Currently Amended) The method, as set forth in claim 23, wherein routing the packet to the one of the plurality of circuit cards comprises:

receiving the packet at a switch; and

switching the packet to ~~the one of the plurality of circuit cards coupled to a~~ predetermined port of the switch coupled to the one of the plurality of circuit cards specified in the routing label.

29. (Currently Amended) The method, as set forth in claim 23, wherein routing the packet to the one of the plurality of circuit cards ~~to~~ comprises:

receiving the packet at a switch; and

switching the packet to the one of the plurality of circuit cards coupled to a predetermined port of the switch as specified by at least a shelf identifier and slot identifier, included in the routing label for transporting the packet.

30. (Previously Presented) The method, as set forth in claim 23, wherein routing the packet to a processor and sending the reply packet comprises:

receiving the packet at a switch;

switching the packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet to the one of the plurality of circuit cards coupled to a second predetermined port of the switch specified by at least a shelf and slot identifiers included in the internal routing label.

31. (Cancelled)

32. (Previously Presented) The method of claim 1, further comprising routing the packet to a processor within the system and sending a reply packet to the one of the plurality of circuit cards specified in the internal routing label in response to the packet type being indicative of a control packet.

33. (Currently Amended) Apparatus at a node of a network, comprising:

a plurality of circuit cards and a switching fabric;

means for receiving a packet, the packet being an IP packet and including a label stack, the label stack including an external routing label for use in forwarding between nodes along a label-switched path;

means for pushing an internal routing label to the label stack of the packet,

means for routing a packet through the switching fabric to one of the plurality of circuit cards based on an internal routing label attached to the packet; and

means for removing the internal routing label prior to transmission of the packet from the apparatus.

34. (Previously Presented) The apparatus of claim 33, further comprising:

a processor,

the processor including means for sending a reply packet in response to receiving a control packet to one of the plurality of circuit cards identified in the internal routing label.

35. (Previously Presented) The node of claim 34, wherein the internal routing label further includes a packet type identifier.

36. (Previously Presented) The apparatus of claim 35 wherein the means for routing also routes based, at least in part, on the packet type identifier.

37. (Previously Presented) The apparatus of claim 35, wherein the means for routing includes means for routing the packet to the processor if the packet type identifier indicates a control packet type.

38. (Previously Presented) The apparatus of claim 33, wherein the internal routing label includes at least one field for identifying the location of one of the plurality of the circuit cards within the node.

39. (Previously Presented) The apparatus of claim 38, wherein the at least one field for identifying the location of one of the plurality of circuit cards within the node includes identifiers for a shelf and a slot of the one of the plurality of circuit cards.

40. (New) The apparatus of claim 33, further comprising memory for storing a routing table, the routing table including fields for the external label and the internal routing label.